WHAT IS CLAIMED IS:

1. A method of controlling a processor comprising switching parallel availability of a plurality of processing blocks formed inside a processor in accordance with a temperature.

2. The method of controlling a processor according to claim 1, comprising switching a combination of the parallel availability and an operating frequency in accordance with a temperature of the processor.

3. The method of controlling a processor according to claim 1, comprising allocating tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

4. The method of controlling a processor according to claim 1 to 3, comprising allocating tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

5. A method of controlling a processor comprising switching between combinations of parallel availability of a

plurality of processing blocks formed inside a processor and an operating frequency by consulting a predetermined table.

6. The method of controlling a processor according to claim 5, wherein the table describes processing performance for each of the combinations.

7. The method of controlling a processor according to claim 6, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, a combination yielding a smaller amount of heat generation than that of a combination selected currently is detected out of the combinations, so that the combination selected currently is switched to the combination detected.

8. The method of controlling a processor according to claim 7, wherein when a plurality of combinations are detected, the combination selected currently is switched to a combination yielding maximum performance.

9. A processor comprising:

a plurality of processing blocks;

a sensor which measures a temperature; and

a control unit which switches parallel availability of the plurality of processing blocks in accordance with the

measured temperature.

10. The processor according to claim 9, wherein the control unit switches between combinations of the parallel availability and an operating frequency in accordance with the temperature.

11. The processor according to claim 9, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

12. The processor according to claim 9 to 11, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

13. A processor comprising:

a plurality of processing blocks;

a table which describes combinations of parallel availability of the plurality of processing blocks and an operating frequency; and

a control unit which consults the table and switches between the combinations as appropriate.

14. The processor according to claim 13, wherein the table describes processing performance for each of the combinations.

15. The processor according to claim 14, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, the control unit selects a combination yielding a smaller amount of heat generation than at present out of the combinations, and switches to the combination selected.

16. An information processing apparatus comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a sensor which measures a temperature; and

a control unit which switches parallel availability of the plurality of processing blocks in accordance with the measured temperature.

17. The information processing apparatus according to claim 16, wherein the control unit switches a combination of the parallel availability and an operating frequency in accordance with the temperature.

18. The information processing apparatus according to claim 16, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

19. The information processing apparatus according to claim 16 to18, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

20. An information processing apparatus comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a table which describes combinations of parallel availability of the plurality of processing blocks and an operating frequency; and

a control unit which consults the table and switches between the combinations as appropriate.

21. An information processing system comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a sensor which measures a temperature; and

a control unit which switches parallel availability of the plurality of processing blocks in accordance with the measured temperature.

22. The information processing system according to claim 21, wherein the control unit switches between combinations of the parallel availability and an operating frequency in accordance with the temperature.

23. The information processing system according to claim 21, wherein the control unit allocates tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

24. The information processing system according to claim 21, wherein the control unit allocates tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

25. An information processing system comprising a processor which executes various tasks,

the processor including:

a plurality of processing blocks;

a table which describes combinations of parallel

availability of the plurality of processing blocks and an operating frequency; and

a control unit which consults the table and switches between the combinations as appropriate.

26. A processor control program comprising switching parallel availability of a plurality of processing blocks formed inside a processor in accordance with a temperature.

27. The processor control program according to claim 26, comprising switching a combination of the parallel availability and an operating frequency in accordance with a temperature of the processor.

28. The processor control program according to claim 26, comprising allocating tasks in consideration of the number of the plurality of processing blocks available in parallel, the number being determined task by task.

29. The processor control program according to claim 26 to 28, comprising allocating tasks to at least a processing block having a lowest temperature among the plurality of processing blocks.

30. A processor control program comprising switching

between combinations of parallel availability of a plurality of processing blocks formed inside a processor and an operating frequency by consulting a predetermined table.